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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,907	07/18/2003	Chao-Chieh Tsai	TS00-299C	5380

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,907	TSAI ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 04 August 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 and 46-95 is/are pending in the application.

4a) Of the above claim(s) 1 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 46-95 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 46-95 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 46-95 are rejected under 35 U.S.C. 102(e) as being anticipated by Tabara(U.S. 6,137,175).

Tabara discloses a semiconductor device with

(46); (62); (77) a substrate (30);

a MOSFET (42A, 42B) on the substrate (30); the MOSFET (42A, 42B) having a source (46S1) and a drain (46D1) and including a silicide portion (38A) over a gate electrode (36A) (see Figures 8-9);

a first ILD layer (48, 124) over the substrate (30) and the MOSFET (42A, 42B) wherein the silicide portion (38A) over the gate electrode (36A) is exposed;

a metal gate portion (52, 130):

over the first ILD layer (48, 124); and

over the silicide portion (38A) over the gate electrode (36A);

the metal gate portion (52, 130) having a width substantially greater than the width of the silicide portion (38A) over the gate electrode (36A) (see Figures 13, 27);

a second ILD layer (138) over the metal gate portion (52, 130) and the first ILD layer (48, 124) (see Figure 29);

a first metal contact (144) through the second ILD layer (138) contacting the metal gate portion (52, 130) (see Figure 31);

a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{xx} deep submicron MOSFET structure (see Figure 31);

whereby the width of the metal gate portion reduces R_g and increases the f_{xx} of the high f_{xx} deep submicron MOSFET structure (20A, 20B) (see Figure 31);

(47); (63) including a dielectric layer: over the substrate and MOSFET but not over the silicide portion over the gate electrode;

under the first ILD layer (see Figure 31);

(48); (64); (79) including a dielectric layer: over the substrate and MOSFET but not over the silicide portion over the gate electrode; between the first ILD layer; the dielectric layer being comprised of SiON (see (see Figure 31);

(49); (65); (80) wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of CoSix, CoSi2; the first ILD layer is comprised of oxide, silicon oxide, USG or TEOS; the metal gate portion is comprised of W, Al, Cu, TiN or Au; the second ILD is comprised of oxide, silicon oxide, HDP or FSG; and the first and second metal contacts are each comprised of W or Cu (see column 8, lines 35-67; column 9, lines 1-67 and column 10, lines 1-64);

(50); (66); (81) wherein the gate electrode is comprised of polysilicon, the silicide portion over the gate electrode is comprised of Cosix; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten; the second ILD is comprised of silicon oxide; and the first and second metal contacts each being comprised of tungsten (see column 8, lines 35-67; column 9, lines 1-67 and column 10, lines 1-64);

(51); (82) wherein the gate electrode has a width of from about 500 to 5000 Å and the metal gate portion has a width of from about 500 to 8000 Å (see column 3, lines 18-42);

(52; (83) wherein the gate electrode has a width of from about 1000 to 3500 Å and the metal gate portion has a width of from about 1000 to 3000 Å (see column 8, lines 35-67);

(53); (84) wherein the gate electrode has a width of about 0.13um and the metal gate portion has a width of from about 1800 to 2400 Å (see column 8, lines 35-67);

(54); (85) wherein the gate electrode has a height of from about 1000 to 3000 Å; the silicide portion over the gate electrode has a thickness of from about 270 to 330 Å; the first ILD layer has a thickness of from about 1700 to 1900 Å; and the metal gate portion has a thickness of from about 1800 to 2200 Å (see column 8, lines 35-67; column 9, lines 1-67 and column 10, lines 1-64);

(55); (86) wherein the gate electrode has a height of from about 1500 to 2200 Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310 Å; the first ILD layer has a thickness of about 1800 Å; and the metal gate portion has a thickness of from about 1900 to 2100 Å (see column 8, lines 35-67; column 9, lines 1-67 and column 10, lines 1-64);

(56); (87) wherein the gate electrode has a height of from about 1500 to 2200 Å; the silicide portion over the gate electrode has a thickness of about 300 Å; the first ILD layer has a thickness of about 1800 Å; and the metal gate portion has a thickness of about 2000 Å (see column 8, lines 35-67; column 9, lines 1-67 and column 10, lines 1-64);

(57) wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion the drain; and wherein the second metal contact contacts the drain silicide portion (see Figure 31);

(58) wherein the MOSFET includes a source Cosix silicide portion over at least a portion of the source and a drain Cosix silicide portion over at least a portion of the

drain; and wherein the second metal contact contacts the drain Cosix silicide portion (see column 8, lines 35-67; column 9, lines 1-67 and column 10, lines 1-64. Figure 31);

(59); (76); (90) wherein the first ILD is planarized (see Figure 31);

(60); (74); (91) wherein the high f_{xx} deep submicron MOSFET structure is positioned within an RF circuit;

(61) wherein the gate electrode has a gate oxide thereunder; the gate oxide having a thickness proximate the source and the drain to significantly reduce the parasitic capacitance and increase the f_{Max} of the high f_{Max} deep submicron MOSFET structure (see Figure 31);

(67) wherein the gate electrode has a width of from about 1000 to 3500 Å and the metal gate portion has a width of from about 1000 to 3000 Å (see column 8, lines 35-67; column 9, lines 1-67 and column 10, lines 1-64);

(68) wherein the gate electrode has a width of about 0.13um and the metal gate portion has a width of from about 1800 to 2400 Å (see column 8, lines 35-67; column 9, lines 1-67 and column 10, lines 1-64);

(69) wherein the gate electrode has a height of from about 1000 to 3000 Å; the silicide portion over the gate electrode has a thickness of from about 270 to 330 Å; the first ILD layer has a thickness of from about 1700 to 1900 Å; and the metal gate portion has a thickness of from about 1800 to 2200 Å (see column 8, lines 35-67; column 9, lines 1-67 and column 10, lines 1-64);

(70) wherein the gate electrode has a height of from about 1500 to 2200 Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310 Å; the

first ILD layer has a thickness of about 1800 Å; and the metal gate portion has a thickness of from about 1900 to 2100 Å (see column 8, lines 35-67; column 9, lines 1-67 and column 10, lines 1-64);

(71) wherein the gate electrode has a height of from about 1500 to 2200 Å; the silicide portion over the gate electrode has a thickness of about 300 Å; the first ILD layer has a thickness of about 1800 Å; and the metal gate portion has a thickness of about 2000 Å (see column 8, lines 35-67; column 9, lines 1-67 and column 10, lines 1-64);

(72) wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain silicide portion (see Figure 31);

(73) wherein the MOSFET includes a source Cosix silicide portion over at least a portion of the source and a drain Cosix silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain Cosix silicide portion (see Figure 31);

(75) wherein the gate electrode has a gate oxide thereunder; the gate oxide having a thickness proximate the source and the drain to significantly reduce the parasitic capacitance and increase the f_{Max} of the high f_{Max} deep submicron MOSFET structure (see Figure 31);

(78) including a dielectric layer: over the substrate and MOSFET but not over the silicide portion over the gate electrode; under the first ILD layer (see Figure 31);

(88) wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain (see Figure 31);

(89) wherein the MOSFET includes a source Cosix silicide portion over at least a portion of the source and a drain Cosix silicide portion over at least a portion of the drain (see Figure 31);

(92) wherein the gate electrode has a gate oxide thereunder;

the gate oxide having a thickness proximate the source and the drain to significantly reduce the parasitic capacitance and increase the f_{Max} of the high f_{Max} deep submicron MOSFET structure (see Figure 31);

(93) further comprising: a second ILD layer over the metal gate portion and the first ILD layer;

a first metal contact through the second ILD layer contacting the metal gate portion;

a second metal contact through the second and first E.D layers contacting the drain completing the formation of the high f_{Max} deep submicron MOSFET structure (see Figure 31);

(94) wherein the first metal contact is a trench contact (see Figure 31);

(95) wherein the second metal contact is a trench contact (see Figure 31).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
October 11, 2005